NAME

chvgpio - Intel Cherry View SoC GPIO controller

SYNOPSIS

device gpio
device chvgpio

DESCRIPTION

chvgpio supports the GPIO controller that can be found in Intel's Cherry View SoC family.

The Cherry View SoC has 5 banks of GPIO pins, NORTH, EAST, SOUTHEAST, SOUTHWEST and VIRTUAL. All but VIRTUAL are exposed to userland as */dev/gpiocN*, where N is 0-3. Pins in each bank are pre-named to match names in the Intel(R) Atomtm Z8000 Processor Series Vol 2

SEE ALSO

gpio(3), gpio(4), gpioctl(8)

Intel(R) Atomtm Z8000 Processor Series Vol 1.

Intel(R) Atomtm Z8000 Processor Series Vol 2.

HISTORY

The **chvgpio** manual page first appeared in FreeBSD 12.

AUTHORS

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