NAME

sume - NetFPGA SUME 4x10Gb Ethernet driver

SYNOPSIS

To compile this driver into the kernel, place the following lines in your kernel configuration file:

device sume

Alternatively, to load the driver as a module at boot time, place the following line in loader.conf(5):

```
if_sume_load="YES"
```

DESCRIPTION

The **sume** driver provides support for NetFPGA SUME Virtex-7 FPGA Development Board with the reference NIC bitstream loaded onto it. The HDL design for the reference NIC project uses the RIFFA based DMA engine to communicate with the host machine over PCIe. Every packet is transmitted to / from the board via a single DMA transaction, taking up to two or three interrupts per one transaction which yields low performance.

There is no support for Jumbo frames as the hardware is capable of dealing only with frames with maximum size of 1514 bytes. The hardware does not support multicast filtering, provides no checksums, and offers no other offloading.

SEE ALSO

arp(4), netgraph(4), netintro(4), ng_ether(4), vlan(4), ifconfig(8)

AUTHORS

The Linux **sume** driver was originally written by Bjoern A. Zeeb. The FreeBSD version and this manual page were written by Denis Salopek as a GSoC project. More information about the project can be found here: https://wiki.freebsd.org/SummerOfCode2020Projects/NetFPGA_SUME_Driver

BUGS

The reference NIC hardware design provides no mechanism for quiescing inbound traffic from interfaces configured as DOWN. All packets from administratively disabled interfaces are transferred to main memory, leaving the driver with the task of dropping such packets, thus consuming PCI bandwidth, interrupts and CPU cycles in vain.

Pre-built FPGA bitstream from the NetFPGA project may not work correctly. At higher RX packet rates, the newly incoming packets can overwrite the ones in an internal FIFO so the packets would arrive in main memory corrupted, until a physical reset of the board.

Occasionally, the driver can get stuck in a non-IDLE TX state due to a missed interrupt. The driver includes a watchdog function which monitors for such a condition and resets the board automatically. For more details, visit the NetFPGA SUME project site.